# PATENT ABSTRACTS OF JAPAN

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(71)Applicant : **RICOH CO LTD**

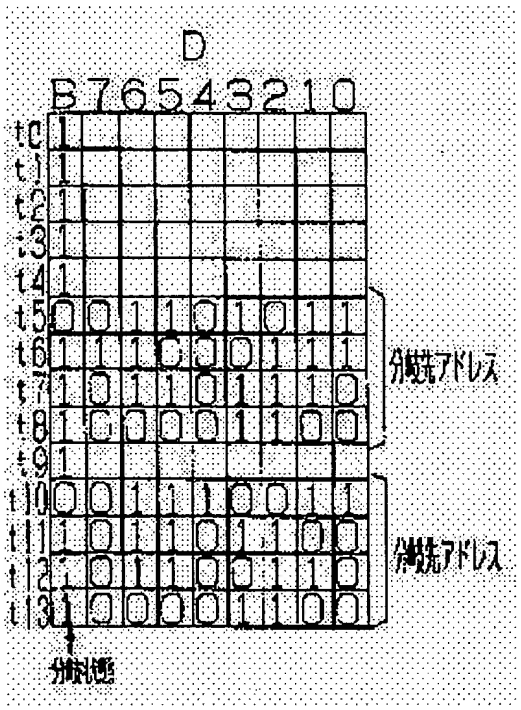
(72)Inventor : **KADOWAKI YUKIO**
**OTEGI SUGITAKA**
**NAKAMURA KEIJI**
**HIRAI TAKAYASU**

## (54) PROCESSOR BUILT-IN TRACE MEMORY

(57)Abstract:

PROBLEM TO BE SOLVED: To trace a fast LSI in real time by dividing a branch destination address by the number of stages of a pipeline and storing the divided branch destination addresses and a specific bit representing branching in a trace memory in a pipeline hazard period.

SOLUTION: The branch destination address is divided by the number of stages of the pipeline and the divided branch destination addresses are stored in the trace memory in the pipeline hazard period. A decision bit for discriminating a branch instruction and a sequential instruction is used in such a way that '0' is stored for the branch instruction and '1' for sequential instruction instead of storing a program address. With the said trace result, many execution histories can be stored by using small memory capacity. Further, a branch source address can easily be specified on an in-circuit emulator(ICE) side by counting the number of '1' of the branch destination address and decision bits.

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